CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of strobe inputs to receive a plurality of strobe signals;

a plurality of data inputs to receive a plurality of data signals transmitted in a transaction in conjunction with said plurality of strobe signals in a source synchronous manner;

bus control logic to produce an externally visible indication that an error has occurred if a glitch on one or more of said plurality of strobe signals is detected.

2. The apparatus of claim 1 wherein said bus control logic is to produce the externally visible indication that the error has occurred by retrying the transaction.

3. The apparatus of claim 1 wherein said bus control logic is to disregard data signals latched in conjunction with said glitch.

4. The apparatus of claim 3 wherein said bus control logic is to initiate said transaction by requesting a data item, and wherein said bus control logic is further to initiate a second transaction to retrieve said data item in response to said glitch being

detected.

5. The apparatus of claim 2 wherein said bus control logic is also, in response said error, to stop sending additional bus requests, and to disregard data received in conjunction with said transaction.

6. The apparatus of claim 5 wherein said bus controller is to retry said transaction after waiting until no further strobes are outstanding.

7. A bus agent comprising:

a plurality of data signal inputs to receive a plurality of data signals;

a plurality of strobe inputs to receive a plurality of strobe signals;

a state machine coupled to receive said plurality of strobe signals and to generate therefrom a plurality of clock signals;

a strobe glitch detection circuit to monitor said plurality of clock signals produced by said state machine to detect glitches on one or more of said plurality of strobe signals.

8. The bus agent of claim 7 wherein said state machine is to receive two complementary strobe signals and to generate therefrom four non-overlapping clock signals, said four non-overlapping clock signals having sequential active periods, and

wherein said strobe glitch detection circuit is coupled to receive two clock signals of said four non-overlapping clock signals, and further wherein said strobe glitch detection circuit is to generate an error signal if a first one of said two clock signals is in an incorrect state at a time determined from the other one of said two clock signals.

9. The bus agent of claim 8 wherein said strobe glitch detection circuit is to generate the error signal if the first one of said two clock signals is in the incorrect state after a delay duration.

10. The bus agent of claim 9 wherein said four non-overlapping clocks have a substantially similar active period, and wherein said delay duration is less than a duration of said active period.

11. The bus agent of claim 7 wherein said plurality of strobe signals is a first set of a first number of strobe signals and wherein said plurality of clocks are a second set of a second number of clocks, said second number being twice the first number, said plurality of clocks being non-overlapping clocks.

12. The bus agent of claim 7 wherein said plurality of data signals comprise a plurality of sets of data signals, each set having an associated strobe and an inverted strobe signal, and wherein said strobe glitch detection circuit comprises a plurality of

strobe glitch detectors, each of said plurality of strobe glitch detectors being coupled to receive a first clock signal and a second clock signal from said plurality of clock signals and to generate a glitch indicator signal if said second clock signal is in an incorrect state after a predetermined duration measured from a transition of the first clock signal.

13. The bus agent of claim 12 wherein each glitch detector comprises:

a delay circuit to receive said first clock signal and to generate a delayed first clock signal;

a latch clocked by said delayed first clock signal, said latch being a falling edge clock triggered latch, said latch having a data input coupled to receive said second clock signal and to generate an output error signal if said second clock signal is absent when a falling edge of the delayed first clock signal clocks the latch.

14. The bus agent of claim 13 wherein said output error signal is further coupled to said latch to retain the output error signal in an active state until a reset signal is received.

15. The bus agent of claim 14 further comprising:

a bus controller to retry a transaction during which a strobe glitch is

detected in response to detection of said strobe glitch.

16. The bus agent of claim 15 wherein said bus controller is also, in response said output error signal, to stop sending additional bus requests, to disregard data received in conjunction with said transaction, and to reset each glitch detector.

17. The bus agent of claim 16 wherein said bus controller is to reset each glitch when no further strobes are outstanding.

18. The bus agent of claim 7 further comprising:

a bus controller to retry a transaction during which a glitch is detected by said strobe glitch detection circuit.

19. A system comprising:

a first bus agent capable of generating data signals and accompanying strobe signals for source synchronous transmission of at least a portion of a transaction;

a second bus agent capable of detecting a glitch on said strobe signals, said second bus agent retrying said transaction in response to the glitch being detected.

20. The system of claim 19 wherein said second bus agent is to disregard data signals latched in conjunction with said glitch.

21. The system of claim 20 wherein said second bus agent is to retry said transaction after waiting until no further strobes are pending.

22. The system of claim 19 wherein said second bus agent is to retry said request without signaling an error or requesting system restart.

23. A method comprising:

receiving a plurality of strobe signals;

generating a plurality of internal clock signals from said plurality of strobe signals;

detecting one of said plurality of internal clock signals being in an incorrect state with respect to another one of said plurality of internal clock signals.

24. The method of claim 23 further comprising:

producing an externally visible signal that an error has occurred.

25. The method of claim 24 wherein producing an externally visible signal that the

error has occurred comprises retrying a data transfer during which the error occurred.

26. The method of claim 23 wherein detecting comprises:

delaying a first internal clock to produce a delayed first internal clock;

latching said second internal clock with said delayed first internal clock to produce an error signal in response to said second internal clock being in the incorrect state when latched by said delayed first internal clock.

27. The method of claim 23 wherein said plurality of internal clock signals have different duty cycles than said strobe signals.

28. A method comprising:

requesting data over a source synchronous bus;

receiving data and a plurality of strobe signals over said source synchronous bus;

detecting a glitch in at least one of said plurality of strobe signals; and

retrying a transaction to retrieve said data.

29. The method of claim 28 further comprising:

waiting until no further strobes are pending to retry said transaction.

30. The method of claim 29 further comprising:

disregarding any data latched in conjunction with said glitch.